

ABSTRACT

A differential transistor pair comprises a plurality of transistor cells in a substrate. Each cell comprises first drain regions at the respective edge of the cell, and a second drain region in between. Source regions are located between the respective first drain region and the second drain region. First gate regions are located between the respective first drain region and the source regions, and second gate regions are located between the source regions and the second drain region. The first drain regions of all cells are interconnected to a common first drain terminal, and the second drain region of all cells are interconnected to a common second drain terminal. The first gate regions of all cells are interconnected to a common first gate terminal, and the second gate regions of all cells are interconnected to a common second gate terminal.